What is claimed is:

1. An integrated circuit comprising

a driver having an output node to be coupled to a conductor external to the integrated circuit, such that the driver launches an initial voltage value on the conductor when the driver changes state; and

a receiver having input hysteresis, the receiver including an input node coupled to the output node of the driver, the input hysteresis having a threshold set such that the initial voltage value does not change an output state of the receiver.

2. The integrated circuit of claim 1 wherein the driver comprises a pullup transistor having an output impedance, and a pulldown transistor having an output impedance, the output impedance of the pullup transistor being greater than the output impedance of the pulldown transistor.

3. The integrated circuit of claim 2 wherein the output impedance of the pullup transistor is at least five times greater than the output impedance of the pulldown transistor.

4. The integrated circuit of claim 1 further comprising:

a simultaneous bidirectional port that includes a data driver and data receiver, the data driver including a closed loop impedance control circuit.

5. The integrated circuit of claim 4 wherein the integrated circuit is a circuit type from the group comprising: a processor, a processor peripheral, a memory, and a memory controller.

6. The integrated circuit of claim 1 wherein the driver includes an input node, and the receiver includes an output node, the integrated circuit further comprising:

a processor coupled to the input node of the driver and to the output node of the receiver, the processor being configured to assert a ready signal on the input node of the driver and to monitor a signal on the output node of the receiver for an indication that the driver and at least one other driver coupled to the input node of the receiver have driven high.

7. The integrated circuit of claim 1 wherein the integrated circuit is a circuit type from the group comprising: a processor, a processor peripheral, a memory, and a memory controller.

8. The integrated circuit of claim 1 further including an initialization circuit to drive an input node of the driver low during initialization.

9. An integrated circuit comprising:

a driver having a pullup transistor and a pulldown transistor with an output node formed at a junction therebetween, the pullup transistor having an output impedance greater than the pulldown transistor; and

a receiver having an input node coupled to the output node of the driver, the receiver having input hysteresis sufficient to detect when the driver and at least one additional driver coupled to the input node drive high.

10. The integrated circuit of claim 9 further comprising:

a simultaneous bidirectional port including at least one initialization circuit; and

a control circuit to turn on the pullup transistor and to turn off the pulldown transistor when the at least one initialization circuit has performed an initialization.

11. The integrated circuit of claim 10 wherein the at least one initialization circuit comprises a closed loop output impedance control circuit.

12. The integrated circuit of claim 10 wherein the at least one initialization circuit includes an output slew rate control circuit.

13. The integrated circuit of claim 10 wherein the integrated circuit is a circuit type from the group comprising: a processor, a processor peripheral, a memory, and a memory controller.

14. A simultaneous bidirectional port circuit comprising:

a data driver having an output impedance control circuit to modify an output impedance of the data driver; and

a synchronization circuit to alert a second simultaneous bidirectional port circuit that the output impedance has been modified.

15. The simultaneous bidirectional port circuit of claim 14 wherein:

the output impedance control circuit is configured to initialize the output impedance of the data driver; and

the synchronization circuit is configured to alert the second simultaneous bidirectional port circuit that the output impedance has been initialized.

16. The simultaneous bidirectional port circuit of claim 15 wherein the synchronization circuit comprises:

a driver having an output node to be coupled through a conductor to an output node of the second simultaneous bidirectional port circuit; and

a receiver having an input node coupled to the output node;

wherein the receiver includes hysteresis sufficient to allow the receiver to change state only after both the output node of the driver and the output node of the second simultaneous bidirectional port circuit are asserted.

17. The simultaneous bidirectional port circuit of claim 16 further including a slew rate control circuit to control the output slew rate of the data driver.

18. The simultaneous bidirectional port circuit of claim 17 wherein the synchronization circuit is configured to assert after the slew rate control circuit is initialized.

19. The simultaneous bidirectional port circuit of claim 14 wherein the synchronization circuit comprises;

a driver having an output node to be coupled to a conductor common to both the simultaneous bidirectional port circuit and the second simultaneous bidirectional port circuit, the driver having a pullup transistor and a pulldown transistor, the pullup transistor having a higher output impedance than the pulldown transistor; and

a receiver having an input node coupled to the output node of the driver.

20. An integrated circuit comprising:

a simultaneous bidirectional port to be coupled to a second simultaneous bidirectional port on a second integrated circuit;

at least one initialization circuit to perform an initialization of the simultaneous bidirectional port; and

a synchronization circuit to be coupled to a second synchronization circuit on the second integrated circuit, to indicate when the initialization of the simultaneous bidirectional data port and an initialization of the second bidirectional port is complete.

21. The integrated circuit of claim 20 wherein the at least one initialization circuit comprises an output impedance control circuit.

22. The integrated circuit of claim 20 wherein the at least on initialization circuit comprises an output slew rate control circuit.

23. The integrated circuit of claim 20 wherein the synchronization circuit comprises:

a driver having an output node to be coupled to an output node of the second synchronization circuit on the second integrated circuit; and

a receiver coupled to the output node of the driver to detect when the output node of the driver and the output node of the second synchronization circuit have signals asserted thereon.

24. An electronic system comprising:

a first integrated circuit having a first simultaneous bidirectional port comprising a first data driver, a first data receiver, a first synchronization driver, and a first synchronization receiver; and

a second integrated circuit having a second simultaneous bidirectional port comprising a second data driver, a second data receiver, a second synchronization driver, and a second synchronization receiver;

wherein output nodes of the first and second data drivers are coupled in common with input nodes of the first and second data receivers, and output nodes of the first and second synchronization drivers are coupled in common with input nodes of the first and second synchronization receivers.

25. The electronic system of claim 24 wherein the first and second simultaneous bidirectional ports include data driver output impedance control circuits, and each of the first and second synchronization drivers are configured to be responsive to a respective one of the data driver output impedance control circuits.

26. The electronic system of claim 24 wherein the first and second synchronization receivers include input hysteresis such that both of the first and second synchronization receivers change state only after both of the first and second synchronization drivers are asserted.

27. The electronic system of claim 24 wherein the first integrated circuit is a circuit type from the group comprising: a processor, a processor peripheral, a memory, and a memory controller.

28. A method of synchronizing an agent to a bidirectional bus comprising:

de-asserting a ready signal to drive a transmission line having a second agent driver present thereon to signify the agent is not ready to communicate on the bidirectional bus;

asserting the ready signal to signify the agent is ready to communicate on the bidirectional bus; and

monitoring the transmission line for an indication that both the agent and the second agent are ready to communicate on the bidirectional bus.

29. The method of claim 28 wherein asserting the ready signal comprises:

turning off a pulldown transistor having a first output impedance; and

turning on a pullup transistor having a second output impedance, wherein the second output impedance is greater than the first output impedance.

30. The method of claim 28 wherein monitoring comprises monitoring an output node of a receiver having input hysteresis.